Monthly Status Report • December 2009
Covering the Period 1 December through 31 December 2009

POWER MEMS DEVELOPMENT

Contract N00014-09-C-0252
Submitted in accordance with Deliverable A001 - Monthly Technical and Financial
SRI Project P19063

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ACTIVITIES AND PROGRESS

MEMS RESETTABLE CIRCUIT BREAKER (TASK 1.1) AND MEMS SWITCH FOR DC-DC VOLTAGE CONVERTERS (TASK 1.2)

Task 1.1 Contributors: Susana Stillwell, Sunny Kedia, Weidong Wang

Task 1.1 Deliverable: 10 prototype packed MEMS-based resettable circuit breakers for testing and analysis in ONR laboratories.

Task 1.2 Contributors: Sunny Kedia, Shinzo Onishi, Scott Samson

Task 1.2 Deliverable: Functional MEMS-based DC-DC converter in a vacuum package.

Task 1.1 and Task 1.2 Progress:

Short Loop Experiments

During this period, we began one short loop experiment to provide data for the flatness of the device silicon (Si) on the silicon-on-insulator (SOI) substrate. To complete this experiment, we processed one double-side-polished (DSP) and one SOI wafer using the same process as full wafer fabrication less the Metal 2, 4, and 5 layers. This process allows us to fabricate the cantilevers as Si-only cantilevers and verify they are flat before silicon dioxide (SiO_2) growth or platinum (Pt) deposition. This short loop is still in process and will be completed at the end of the period.

Fabrication

During this period, we began a repeat of the full wafer fabrication discussed in previous reports using one SOI and one DSP substrate. We also revised the process flow to include changes based on information gathered from the first full wafer fabrication and the finite element analysis (FEA) modeling results. These changes included a change of the heater material stack for the Task 1.1 circuit breaker and a change in the indent layer thickness. The SiO_2 on the heater will be changed to silicon nitride (Si_3N_4), a tensile film that will cause a bending in the downward direction after release, opposite to the upward bend produced with the compressive SiO_2. The increase to the indent layer will help keep the cantilever from touching the bottom substrate. We will begin processing wafers following this process flow by the end of the period.

Finite Element Modeling

We set up an FEA model for the MEMS cantilever of the DC-DC switch and performed structural analysis using the model. The simulation result shows that the cantilever tip bends down for about 1 μm, considering initial film stresses of -350 MPa for the SiO_2 layer and 100 MPa for the Au and Pt layers, as shown in Figure 1. This agrees with the experimental result. Thus, an increase of the indent layer thickness will help keep the cantilever tip from touching the bottom substrate after release.

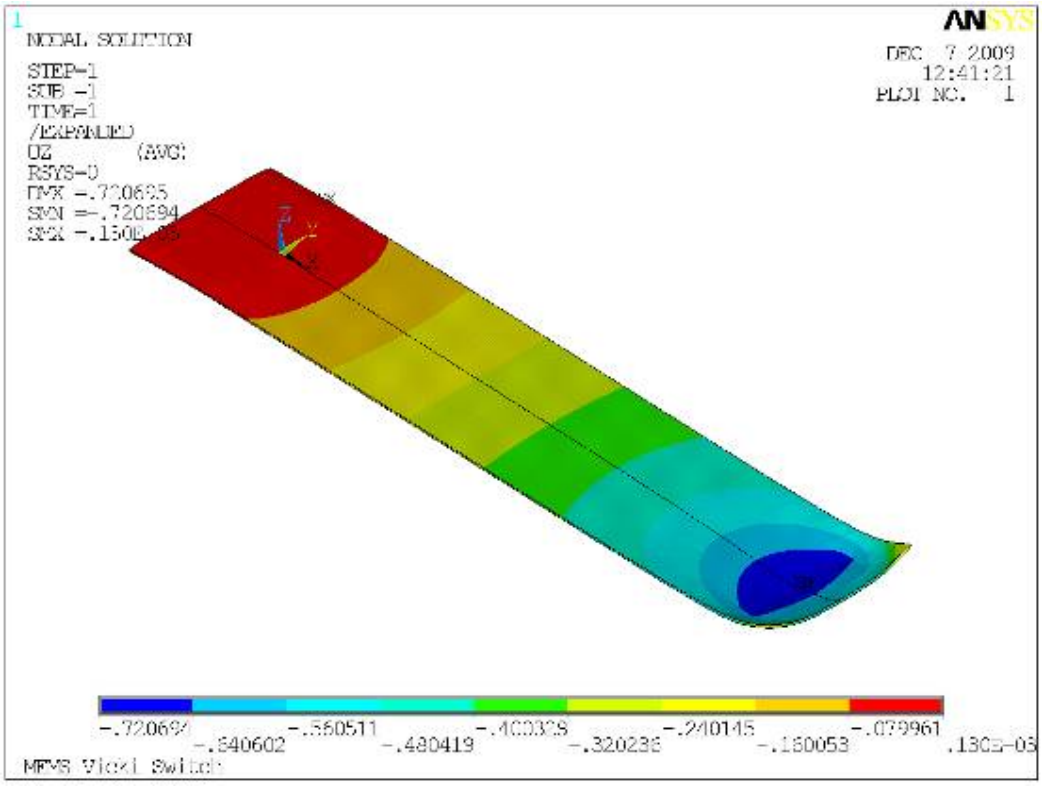

Figure 1: FEA for DC-DC cantilever.

DIAMOND HEAT SPREADER OR HEAT SINK FOR HIGH-POWER MEMS SWITCH APPLICATIONS (TASK 1.3)

Contributors: Priscila Spagnol, Shinzo Onishi, Drew Hanser, John Bumgarner

Deliverable: Prototype device fabricated on a thin-film diamond heat spreader layer and individual samples of diamond on Si or other suitable substrates for material evaluation.

Progress:

During this period we were able to deposit one free-standing microcrystalline diamond film (~220 µm) with reduced stress that did not break or crack after the back Si etch removal. The structure used was composed of a 3-mm Si (100) substrate, 6-µm LPCVD SiO_2, ~2-µm nanocrystalline diamond film grown using the heated stage, and finally the thick microcrystalline diamond film grown on the cooled stage. We are currently repeating the same deposition conditions to check reproducibility of the growth stack.

Thermal conductivity measurement using 3 ω method. We have experienced three major problems with our previous setup for the measurement:

- The signal recovery lock-in amplifier has some limitations at low end frequencies.
- Probes are too sensitive against E-M noises and vibrations to adjust null of the bridge.
- Supplying alternate power to heater/sensor wires may be too low to overcome noise.

Our solutions were as follows:

- Increased the time constant of the lock-in amplifier to 1 second.
- To secure connections, wire bonder and silver paint were used instead of the probe station.
- Used shorter heater/sensor wires and increased power density on the wires.
- Use simple circuit, two-terminal bridge for finding solutions.

Preliminary Results. The output of the lock-in amplifier is far smaller and more stable. In the results, we have better control of the excess noise. Thermal conductivity (TC), κ_s, calculated from the graph in Figure 2, was 200 [$W \cdot K^{-1} \cdot m^{-1}$]. The TC may be too high; however, the thermal conductivity may be smaller after removal of the end effect using four terminals to the heater/sensor wire.

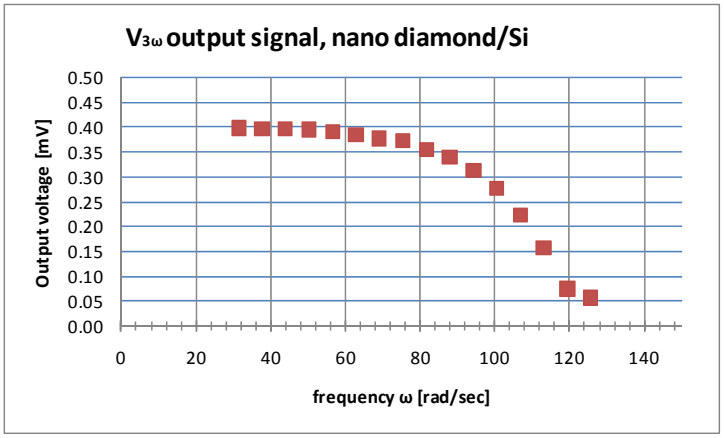

Figure 2: $V_{3\omega}$ output voltage over frequency [rad/s].

Thermal conductivity of a sample consisting of 50 nm SiO_2 on silicon substrate was 132 [$W \cdot K^{-1} \cdot m^{-1}$] with the same setup. The value is comparable with the literature, 152 [$W \cdot K^{-1} \cdot m^{-1}$] without SiO_2 layer. We are ready to measure more samples with four terminals to the heater/sensor wire.

POSITRON TRAPPING AND STORAGE (TASK 2)

Contributors: Ashish Chaudhary, Friso van Amerom, Tim Short

Deliverable: A minimum of four MEMS-based trap structures for RF trapping of electrons

Progress:

First Fabrication Run

We successfully completed the first fabrication run and identified several critical issues to resolve. One of the failures was the use of "cool grease," a commercial high heat conductivity grease to adhere a product wafer to a carrier wafer while performing deep reactive ion etching that might punch through and vent the backside He cooling gas. On these wafers, after acetone soak to remove the carrier wafer, the ZnO layer was discolored in several locations as shown in Figure 3. SEM analysis of the discolored ZnO layer indicated that it was semi-insulating, which would cause surface charging in the electron trap that might interfere with electron trapping due to charge repulsion.

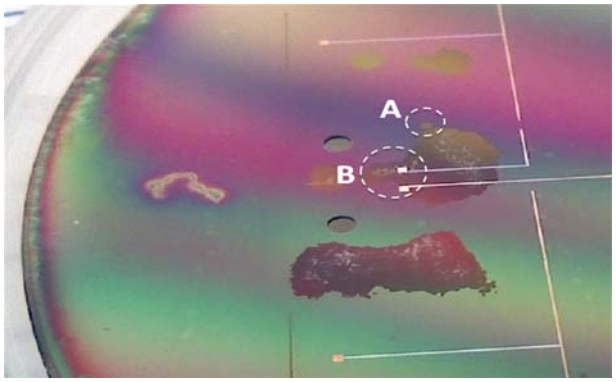

Figure 3: Spots on the device wafer where ZnO layer was discolored. Spot A has discoloration while spot B has discoloration and some cool grease residue.

The process was duplicated with a second wafer, except that this time we used no carrier wafer during the DRIE process. Through-wafer etch was successfully done without any damage to the (Si_3N_4 + SiO_2) membranes and without He leakage that would shut down the process tool. It is expected that the remaining fabrication of the current wafer will be completed by 23 December.

Test Setup

Most of the test setup components have been received.

FINANCIAL STATUS

R&D Status Report

Program Financial Status

15 July 2009 through 12 December 2009

Contract Item No.	Current Funding	Current Period Expenses	Cumulative Expenses	% Budget Complete
0001	$1,829,849	$74,917	$459,552	25%
Project Commitments		(432)	258,077	
Total	$1,829,849	$74,485	$717,629	

Based on currently authorized work:

Is current funding sufficient for the current fiscal year (FY)? (Explain if NO) **Yes**

What is the next FY funding requirement at current anticipated levels **N/A** (**base fully funded)**